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Parallel Circuit Simulation: A Historical Perspective and Recent Developments

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Abstract

Transistor-level circuit simulation is a fundamental computer-aided design technique that enables the design and verification of an extremely broad range of integrated circuits. With the proliferation of modern parallel processor architectures, leveraging parallel computing becomes a necessity and also an important avenue for facilitating large-scale circuit simulation. This monograph presents an in-depth discussion on parallel transistor-level circuit simulation algorithms and their implementation strategies on a variety of hardware platforms. While providing a rather complete perspective on historical and recent research developments, this monograph highlights key challenges and opportunities in developing efficient parallel simulation paradigms.

Contents

1

Introduction

As one of the most critical forms of pre-silicon simulation and verification, transistor-level circuit simulation (e.g., SPICE) is essential for the design of a very broad range of integrated circuits and systems such as custom digital integrated circuits (ICs), memories, analog, mixed-signal, and radio-frequency (RF) designs [74]. Circuit simulation serves the critical mission of predicting circuit performance and makes it possible to disqualify a failing design for expensive chip fabrication. Equally, if not more importantly, the ability of predicting circuit performance through simulation is at the core of any design process; it makes the implementation of complex integrated circuits technically feasible and economically viable while relaxing any heavy need for prototyping.

As a fundamental design and verification enabler, circuit simulation has been under a long-lasting active development since the dawn of the semiconductor industry [10, 62, 70, 71, 73, 74, 83, 102, 105, 114]. However, circuit simulation does not come without cost. Several decades ago, when computer hardware and CPU time were both precious commodities, large-scale circuit simulation was an expensive necessity [83]. To date, designers have the access to much cheaper and more powerful computing facilities, thanks to the remarkable growth of

the semiconductor industry in the past decades. Some form of circuit simulation is almost indispensable for any IC design flow. Electronic circuit simulation techniques have even diffused into other disciplines for purposes such as predicting the behavior of biological systems [67].

1.1 Historical and Recent Technological Drivers for Parallel Circuit Simulation

While a wealth of simulation methods and tools have been crafted to serve many different simulation needs, there is an unsaturated demand for higher accuracy, faster speed, and new analysis capabilities in simulation as the designers strive to deliver increasingly complex IC designs with more functionality and improved performance. Simulation of large IC designs with increasingly complex device models, necessary for modeling modern fabrication processes, remains as a significant challenge. It is by no means surprising that circuit designers may have to spend days, weeks, or even months of CPU time to perform expensive transistor-level circuit simulation. As such, simulation is one of the most critical bottlenecks in the current design flow. Insufficient simulation limits the extent to which pre-silicon verification and design space exploration may be conducted, contributing to long design turnaround time, sub-optimal designs, and even chip failures.

To this end, it is logical not only to develop efficient simulation algorithms but also to leverage parallel computing to enable large-scale circuit simulation. It is also not surprising that *parallel circuit simulation* is not a new concept. There have been earlier attempts to develop parallel simulation capabilities on vector machines, multiprocessors, and supercomputers, either custom built or commercially available [12, 13, 18, 51, 98, 112, 118, 125].

On the other hand, the recent industry's shift to multi- and many-core processor technology has literally made every modern-day desktop, server, and laptop a parallel computing system [3, 8, 25, 34, 36, 45, 50, 64, 72, 85, 96, 109, 116]. This shift toward chip multiprocessors (CMPs) reflects the fundamental performance and power tradeoffs in lieu of VLSI technology scaling. In addition, commodity many-core graphics processing units (GPUs) [4, 77, 78] and heterogeneous

processors [2, 86] with impressive computing power have also merged. For instance, modern GPUs may integrate hundreds of streaming processors on-chip, deliver a peak performance of hundreds of GFLOPS to several TFLOPS, and have a memory bandwidth exceeding 100 GB/s [4, 78]. User-friendly programming model and interfacing tools have also merged for developing general-purpose applications on GPUs [77].

1.2 New Challenges and Opportunities of Parallel Circuit Simulation

This change of the computing landscape has produced profound implications on how compute-intensive applications shall be developed. It has also sparkled active new research activities on parallel circuit simulation. The motivations behind this renewed interest in parallel circuit simulation are multifold.

As power consumption acts as a show stopper for continuing scaling the clock frequency, the performance of single-threaded applications quickly saturates. Simply put, the software developer's "free ride" of the Moore's Law is coming to an end. Further improvement of software performance may only come from explicit exploration of parallelism [6]. To certain extent, this fact has forced the researchers and practitioners to more seriously look into parallel simulation. More importantly, it has stimulated active and exciting development of modern commercial parallel circuit simulators from all major EDA tool vendors and across the industry (see e.g., [1, 32, 110]), and provided impetus for new research in parallel circuit simulation and other areas of parallel electronic design automation [11].

On the other hand, advancements in CMOS and processor technologies have made parallel computing ubiquitous. Modern multi- or many-core processors offer an amount of compute power that was even hardly available on bulky and expensive mainframes and supercomputers decades ago. Today, affordable terascale parallel compute power is at the disposal of typical circuit designers. As illustrated in Figure 1.1, a diverse spectrum of parallel hardware platforms exists, ranging from CMPs, heterogeneous processors, hardware accelerators (GPUs and FPGAs), and SMPs to computer clusters and supercomputers. Each

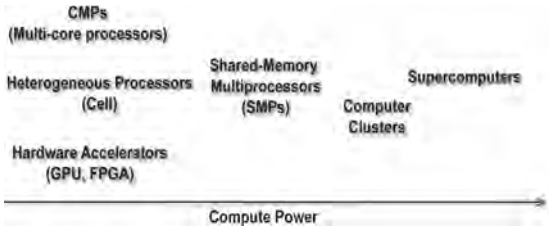

Fig. 1.1 Parallel compute hardware platforms.

compute node of present day clusters and supercomputers may include one or several multicore processors and even attached accelerators such as GPUs. As such, leveraging the ubiquitously available parallel compute hardware is a natural step for addressing the computational challenges of large-scale circuit simulation.

It is noteworthy that modern parallel processor architectures have the potential to enable circuit simulation approaches that are more massively parallel than explored ever before. For instance, on-chip interconnect networks in multicore processors are significantly advantageous over the off-chip interconnects in conventional multichip SMP (symmetrical multiprocessing) processors. On-chip interconnects span smaller distances and hence incur far less latency and power consumption. On-chip buses can be made much wider than those on a PCB. As a result, core-to-core and core-to-memory bandwidths and latencies in multicore processors are orders of magnitude better than those of SMPs, enabling finer grained parallelism. Computer clusters consisting of interconnected multicore processors can provide a greater amount of compute power, leveraged based upon a combination of chip-multiprocessing and distributed processing.

Moreover, the emergence of modern commodity heterogeneous platforms, comprising homogenous multicore microprocessors with attached accelerators (e.g., GPUs) or "fused" heterogeneous cores on the same die [2, 86], brings appealing new opportunities to the computing landscape. Impressive speedups may be gained if the workload is optimally partitioned, and the resulting partitioned tasks are efficiently processed on distinct (e.g., general-purpose vs. SIMD) processing cores that match each task's characteristics.

However, challenges still exist as we attempt to leverage this diverse spectrum of modern processor platforms for parallel circuit simulation. One central challenge, which is possibly long lasting, lies in the difficulty of scaling parallel simulation performance up to large numbers of processors due to the existence of unavoidable parallel overheads. To this end, it is essential to explore a plethora of new algorithmic and implementation level innovations that identify and exploit rich and orthogonal forms of parallelism in circuit simulation. It is desirable to exploit diverse (e.g., both task and data) parallelism with varying parallel granularity, synchronization overhead, and data movement patterns to fully utilize the available parallel compute power, and/or determine the best use of a particular type of processing units of a heterogeneous platform. The above considerations also underscore the important roles played by hardware characteristics (e.g., number and types of processors, cache size, memory bus bandwidth, and latency) and prompt algorithm/hardware interactions during the process of parallel algorithm design.

Looking in a different angle, we shall note that circuit properties have a definitive influence on the performance of a given simulation algorithm. In many ways, today's IC designs look different from older designs that were targeted during the early developmental phase of parallel simulation technologies several decades ago. In scaled fabrication processes, MOS transistors possess many more non-ideal device effects that must be included in transistor models and captured in simulation. We also see an explosion of design complexity, which is reflected not only by escalating device count but also by significantly increased parasitic coupling. Both factors stress the existing circuit simulation methodologies by creating large, complex, and highly coupled simulation instances. The desire toward accurate full-chip verification challenges the existing simulation technologies at yet another higher level, where a mixture of digital, analog, and memory blocks must be feasibly simulated.

While it is anticipated that "going for parallel" may offer an outstanding opportunity to tackle the above simulation challenges, it is observed that the ongoing technology and design trends clearly steer simulation technologies toward delivering higher performance,

improved robustness, and accuracy. Nevertheless, these trends have broken the underlying assumptions of some classical parallel simulation techniques, rendering them less attractive or inapplicable for modern chip designs. This, however, strongly motivates the development of new parallel simulation approaches that are optimized for current IC designs in order to meet the desired performance, robustness, and accuracy requirements.

1.3 Focus and Organization of This Article

Circuit simulation is a broad field. Over the years, a myriad of simulation approaches have emerged, delivering solutions for a wide variety of digital, analog, mixed-signal, RF, and memory circuits as well as full-chip simulation needs with varying performance and accuracy targets. Clearly, examining all this large body of work from a parallel perspective is simply infeasible, given the scope limitation of this monograph.

As such, the main focus of this monograph is placed upon parallel transistor-level simulation techniques aimed at delivering full-SPICE accuracy. A comprehensive review, which is not meant to be exhaustive, is devoted to significant early developments in the past decades, and more recent work that has been stimulated by the arrival of the multicore computing era.

For the sake of completeness, key concepts behind fast-SPICE are succinctly reviewed to provide a basic exposure to the accuracy-performance tradeoffs made in this line of simulation techniques, which present a significant ongoing industrial development [1, 26, 32]. Elements of fast-SPICE techniques are contrasted with some of historical parallel simulation techniques.

The rest of this monograph is organized as follows. In Section 2, to set up a stage for this review, existing parallel circuit simulation works are classified according to two different views, *algorithmic level of parallel processing* and the *domain of parallel processing*. The two views offer a systematic examination of the types of parallelism that may be exploited in circuit simulation. Parallel direct simulation methods and the implementation issues are discussed in Section 3. Section 4 is devoted to two special classes of domain decomposition-based parallel

simulation methods, nonlinear relaxation methods and waveform relaxation, which were the subjects of many historical research efforts. Other linear and nonlinear domain decomposition methods are presented in Sections 5 and 6, respectively. Some recent efforts in exploiting advanced numerical integration techniques for parallel simulation are described in Section 7. A multialgorithm parallel simulation framework, leveraging coarse-grained interalgorithm parallelism, is presented in Section 8. A succinct review of fast-SPICE is given in Section 9.

For most part of the aforementioned sections, the assumed underlying hardware architecture is general-purpose MIMD machine (e.g., multicore processors or computer clusters), which cover the bulk of previous and ongoing parallel simulation work. Some of the reviewed historical work was conducted on traditional vector machines.

Recent research activities on leveraging modern hardware accelerators and heterogeneous processors are reviewed in Section 10. Finally, confusions are drawn in Section 11.

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